LMP91200 Configurable AFE for Low-Power Chemical Sensing Applications

Check for Samples: LMP91200

FEATURES

- **Programmable Output Current in Temperature Measurement**
- **Programmable Output Common Mode Voltage**
- **Active Guarding**
- **On Board Sensor Test**
- **Supported by Webench Sensor AFE Designer**
- **Supported by Webench Sensor Designer Tools**

APPLICATIONS

- **pH Sensor Platforms**

KEY SPECIFICATIONS

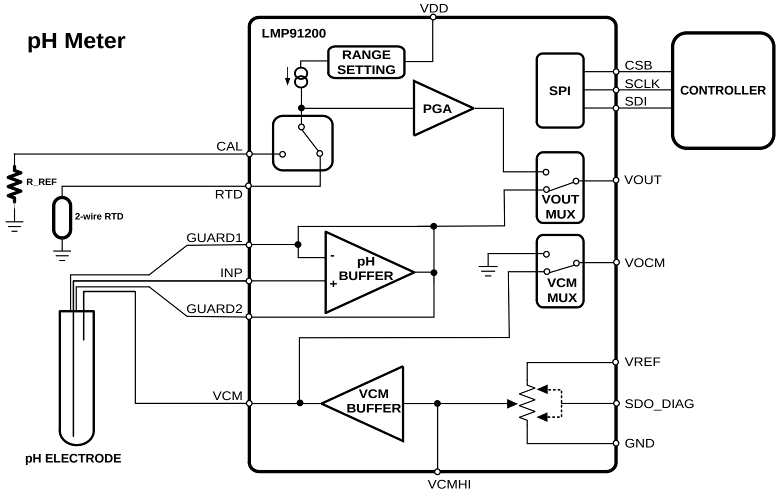
Unless otherwise noted, typical values at T_A = 25°C, V_S=(VDD-GND) = 3.3V

- **pH Buffer Input bias current (0<V_{INP} <3.3V)**
  - **max @ 25°C: ±125 fA**
  - **max @ 85°C: ±445 fA**
- **pH Buffer Input bias current (-500mV<V_{INP}-V_{CM} <500mV), V_S=(VDD-GND)=0V**
  - **max @ 25°C: ±600 fA**
  - **max @ 85°C: ±6.5 pA**
- **pH Buffer Input offset voltage: ±200 µV**
- **pH Buffer Input offset voltage drift: ±2.5 µV/°C**
- **Supply current (pH mode): 50 µA**
- **Supply voltage: 1.8 V to 5.5 V**
- **Operating temperature range: -40°C to 125°C**
- **Package: 16-Pin TSSOP**

DESCRIPTION

The LMP91200 is a configurable sensor AFE for use in low power analytical sensing applications. The LMP91200 is designed for 2-electrode sensors. This device provides all of the functionality needed to detect changes based on a delta voltage at the sensor. Optimized for low-power applications, the LMP91200 works over a voltage range of 1.8V to 5.5V. With its extremely low input bias current it is optimized for use with pH sensors. Also in absence of supply voltage the very low input bias current reduces degradation of the pH probe when connected to the LMP91200. The Common Mode Output pin (VOCM) provides a common mode offset, which can be programmed to different values to accommodate pH sensor output ranges. For applications requiring a high impedance common mode this option is also available. Two guard pins provide support for high parasitic impedance wiring. Support for an external Pt1000, Pt100, or similar temperature sensor is integrated in the LMP91200. The control of this feature is available through the SPI interface. Additionally, a user controlled sensor diagnostic test is available. This function tests the sensor for proper connection and functionality. Depending on the configuration, total current consumption for the device is 50µA while measuring pH. Available in a 16-pin TSSOP package, the LMP91200 operates from -40°C to +125°C.

Typical Application



Connection Diagram

16-Pin TSSOP

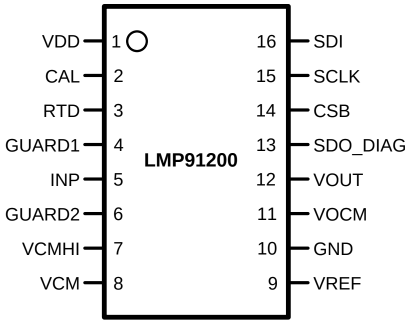


Figure 1. Top View

PIN DESCRIPTIONS

Pin	Name	Description
1	VDD	Positive Power Supply
2	CAL	Connect an external precision resistor here for purpose of temperature measurement calibration
3	RTD	Pt100/Pt1000 input / internal current source output
4	GUARD1	Active guard pin
5	INP	Non-inverting analog input of pH buffer
6	GUARD2	Active guard pin
7	VCMHI	High Impedance Programmable Common Mode output
8	VCM	Buffered Programmable Common Mode output
9	VREF	Voltage reference input
10	GND	Analog ground
11	VOCM	Output common mode voltage
12	VOUT	Analog Output
13	SDO_DIAG	Serial Data Out /Diagnostic enable
14	CSB	Chip select, low active.
15	SCLK	Serial Clock
16	SDI	Serial Data In

Absolute Maximum Ratings (1) (2) (3)

ESD Tolerance (4)	Human Body Model	2000V
	Machine Model	150V
	Charge Device Model	1000V
Supply Voltage (V_S = VDD-GND)		-0.3V to 6.0V
Voltage between any two pins		-0.3V to VDD+0.3V
Current out at any pin		5mA
Storage Temperature Range		-65°C to 150°C
Junction Temperature (5)		+150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not specified. For ensured specifications and the test conditions, see the Electrical Characteristics Tables.
(2) For soldering specifications see product folder at www.ti.com and SNOA549
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(5) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

Operating Ratings (1)

Supply Voltage (V_S=VDD-GND)		1.8V to 5.5V
Temperature Range		-40°C to 125°C
Package Thermal Resistance (θ_{JA} (2))	16-Pin TSSOP	31°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not specified. For ensured specifications and the test conditions, see the Electrical Characteristics Tables.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

Electrical Characteristics(1)(2)(3)

Unless otherwise specified, all limits specified for T_A = 25°C. V_S=(VDD-GND)=3.3V. VREF=3.3V. Boldface limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min(4)	Typ(5)	Max(4)	Units
Power supply						
Is	Supply Current(6)(7)	pH measurement mode		50	54 **59**	µA
		Temperature measurement mode, I_{CS}=100uA		300	325 **330**	
		Temperature measurement mode, I_{CS}=200uA		400	432 **437**	
		Temperature measurement mode, I_{CS}=1000uA		350	364 **372**	
		Temperature measurement mode, I_{CS}=2000uA		470	477 **477**	
pH Buffer						
Aol$_{pH}$	Open loop Gain	INP=1.65V, 300mV = VOUT = VDD-300mV	**90**	120		dB
Vos$_{pH}$	Input Voltage Offset(6)	INP=1/8VREF	-200 **-350**		200 **350**	µV
		INP=7/8VREF	-200 **-350**		200 **350**	
TcVos$_{pH}$	Input offset voltage drift(8)(9)	INP=1/8VREF	-2.5		2.5	uV/°C
		INP=7/8VREF	-2.5		2.5	
VOS$^{pH\_drift}$	Long term V_{OSpH} drift(10)	500 hours OPL		150		µV
Ib$_{pH}$	Input bias current at INP(9)	0V<INP<3.3V	-125		125	fA
		0V<INP<3.3V, 85°C	-445		445	fA
		0V<INP<3.3V, 125°C	-1.5		1.5	pA
		-500mV<(INP-VCM)<500mV, V_S=0V.	-600		600	fA
		-500mV<(INP-VCM)<500mV, 85°C, V_S=0V.	-6.5		6.5	pA
		-500mV<(INP-VCM)<500mV, 125°C, V_S=0V.	-100		100	pA
GBWP$_{pH}$	Gain Bandwidth Product(9)	C_L=10pF, R_L=1Mohm		220		KHz
CMRR$_{pH}$	DC_Common mode rejection ratio	1/8VREF<INP<7/8VREF	80			dB
PSRR$_{pH}$	DC_Power supply rejection ratio	1.8V<VDD<5V INP=1/8VREF	80			dB
		1.8V<VDD<5V INP=7/8VREF	80			
En_RMS$_{pH}$	Input referred noise (low frequency)(9)	Integrated 0.1Hz to 10Hz		2.6		µV_{PP}

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(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that TJ = TA. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where TJ >TA.
(2) Positive current corresponds to current flowing into the device.
(3) The voltage on any pin should not exceed 6V relative to any other pins.
(4) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using the Statistical Quality Control (SQC) method.
(5) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
(6) Boldface limits are production tested at 125°C. Limits are specified through correlations using the Statistical Quality Control (SQC) method.
(7) Excluding all currents which flows out from the device.
(8) Offset voltage average drift is determined by dividing the change in V_{OS} at the temperature extremes by the total temperature change.
(9) This parameter is specified by design and/or characterization and is not tested in production.
(10) Offset voltage long term drift is determined by dividing the change in V_{OS} at time extremes of OPL procedure by the length of the OPL procedure. OPL procedure: 500 hours at 150°C are equivalent to about 15 years.

Electrical Characteristics(1)(2)(3) (continued)

Unless otherwise specified, all limits specified for T_A = 25°C. V_S=(VDD-GND)=3.3V. VREF=3.3V. Boldface limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min(4)	Typ(5)	Max(4)	Units
en$_{pH}$	Input referred noise (high frequency)(9)	f=1kHz		90		nV/√Hz
Isc$_{pH}$	Output short circuit current(11)	Sourcing, Vout to GND, INP=1.65V	**10**	13		mA
		Sinking, Vout to VDD, INP=1.65V	**8**	12		mA
VCM Buffer						
VCMHI_acc	VCMHI accuracy		-1.6		1.6	mV
Tc_VCMHI	VCMHI temperature coefficient(9)(12)	-40°C<T_A<125°C	-18	-5	8	µV/°C
VCMHI_acc_VREF	VCMHI_acc vs. VREF(9)(13)	1.8V<VREF<5.0V	-500	-100	300	µV/V
Rout$_{VCMHI}$	VCMHI Output Impedance(9)	VCMHI=1/2 VREF		250		KΩ
Aol$_{VCM}$	Open loop Gain(6)	VCMHI=1/2 VREF, 300mV<VCM<VDD-300mV	**90**	120		dB
Vos$_{VCM}$	(VCM-VCMHI)(6)	VCMHI=1/8 VREF	-200 **-350**		200 **350**	µV
		VCMHI=7/8 VREF	-200 **-350**		200 **350**	
TcVos$_{VCM}$	Input offset voltage drif ot (VCM-VCMHI)(8)(9)	VCMHI=1/8 VREF	-2.5		2.5	µV/°C
		VCMHI=7/8 VREF	-2.5		2.5	
Zout$_{VCM}$	Output Impedance(9)	f=1KHz		4		Ω
PSRR$_{VCM}$	DC_Power supply rejection ratio	1.8V<VDD<5V, VCMHI=1/8VREF	80			dB
		1.8V<VDD<5V, VCMHI=7/8VREF	80			
En_RMS$_{VCM}$	Input referred noise (low frequency)(9)	Integrated 0.1Hz to 10Hz		2.6		µV$_{PP}$
en$_{VCM}$	Input referred noise (high frequency)(14)	f=1KHz		90		nV/√Hz
Isc$_{VCM}$	Output short circuit current(15)	Sourcing, Vout to GND VCMHI=1/2VREF	**10**	16		mA
		Sinking, Vout to VDD VCMHI=1/2VREF	**8**	12		
Current Source						
I$_{CS}$	Current Source I_{CAL}, I_{RTD}	Programmable current		100 200 1000 2000		µA
In_RMS$_{CS}$	Input referred noise (low frequency)(14)	Integrated 0.1Hz to 10Hz		33		nA$_{PP}$
in$_{CS}$	Input referred noise (high frequency)(14)	f=1KHz		120		pA/√Hz
TcI$_{CS}$	Current Source drift(14)(16)		-200	±35	200	ppm/°C
I_acc$_{CS}$	Current Source accuracy		**-2.5**	1	**2.5**	%

(11) The short circuit test is a momentary open loop test.
(12) VCMHI voltage average drift is determined by dividing the change in VCMHI at the temperature extremes by the total temperature change.
(13) VCMHI_acc vs. VREF is determined by dividing the change in VCMHI_acc at the VREF extremes by the total VREF change.
(14) This parameter is specified by design and/or characterization and is not tested in production.
(15) The short circuit test is a momentary open loop test.
(16) Current source drift is determined by dividing the change in I_{CS} at the temperature extremes by the total temperature change.

Electrical Characteristics[1][2][3] (continued)

Unless otherwise specified, all limits specified for T_A = 25°C. V_S=(VDD-GND)=3.3V. VREF=3.3V. Boldface limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min[4]	Typ[5]	Max[4]	Units
PGA						
Vos_{PGA}	Input Voltage Offset[17]	+IN_PGA (Internal node) = 500mV	-275 **-480**		275 **480**	µV
$TcVos_{PGA}$	Input offset voltage drift[18][19]	+IN_PGA (Internal node) = 500mV	-2.5		2.5	uV/°C
Aol_{PGA}	Open loop Gain	+IN_PGA (Internal node) = 500mV	**90**	120		dB
Av_{PGA}	Gain	Programmable gain		5 10		V/V
Av_acc_{PGA}	Gain accuracy		**-1.3**		**1.3**	%
En_RMS_{PGA}	Input referred noise (low frequency)[18]	Integrated 0.1Hz to 10Hz		2.6		μV_{PP}
en_{PGA}	Input referred noise (high frequency)[18]	f=1KHz		90		nV/√Hz
$PSRR_{PGA}$	DC_Power supply rejection ratio	1.8V<VDD<5V, +IN_PGA (Internal node) = 500mV	80			dB
Isc_{PGA}	Output short circuit current[20]	Sourcing, Vout to GND +IN_PGA (Internal node) = 500mV	**10**	16		mA
		Sinking, Vout to VDD +IN_PGA (Internal node) = 500mV	**8**	12		
Reference Input						
Rin_{VREF}	Input impedance[18]			500		KΩ

(17) Boldface limits are production tested at 125°C. Limits are specified through correlations using the Statistical Quality Control (SQC) method.
(18) This parameter is specified by design and/or characterization and is not tested in production.
(19) Offset voltage average drift is determined by dividing the change in V_{OS} at the temperature extremes by the total temperature change.
(20) The short circuit test is a momentary open loop test.

Electrical Characteristics (Serial Interface)[1]

Unless otherwise specified. All limits specified for T_A=25°C, V_S=(VDD-GND)=3.3V.

Symbol	Parameter	Condition	Min[2]	Typ[3]	Max[2]	Units
VIL	Logic Low Threshold				0.3XVDD	V
VIH	Logic High Threshold (SDO pin)		0.7XVDD			V
VOL	Output Logic LOW Threshold (SDO pin)	ISDO=100µA			0.2	V
		ISDO=2mA			0.4	
VOH	Output Logic High Threshold	ISDO=100µA	VDD-0.2			V
		ISDO=2mA	VDD-04			
t1	High Period, SCLK	See[4]	100			ns
t2	Low Period, SCLK		100			ns
t3	Set Up Time, CSB to SCLK		50			ns
t4	Set Up Time, SDI to SCLK		30			ns
t5	Hold Time,S CLK to SDI		10			ns
t6	Hold Time,SCLK to SDO_DIAG		40			ns
t7	Hold Time, SCLK Transition to CSB Rising Edge		50			ns

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that TJ = TA. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where TJ >TA.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using the Statistical Quality Control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
(4) Load for these tests is shown in the timing diagram test circuit.

Electrical Characteristics (Serial Interface)(1) (continued)

Unless otherwise specified. All limits specified for T_A=25°C, V_S=(VDD-GND)=3.3V.

Symbol	Parameter	Condition	Min(2)	Typ(3)	Max(2)	Units
t8	CSB Inactive	See(4)	50			ns
t9	Hold Time, SCLK Transition to CSB Falling Edge		10			ns
t_R/t_F	SDO_DIAG Signal Rise and Fall Times	Diagnostic disabled(4)(5)		30		ns

(5) This parameter is specified by design and/or characterization and is not tested in production.

Electrical Characteristics (Diagnostic)(1)

Unless otherwise specified. All limits specified for T_A=25°C, V_S=(VDD-GND)=3.3V.

Symbol	Parameter	Condition	Min(2)	Typ(3)	Max(2)	Units
DIAG_t_{SET}	SDO_DIAG setup time(4)			200		ns
DIAG_t_R/DIAG_t_F	Diagnostic Rise and Fall Times (Signal at SDO_DIAG pin, in Diagnostic Mode)(4)			30		ns
DIAG_t_{ON}	Minimum t_{ON} of the diagnostic pulse at SDO_DIAG pin in Diagnostic Mode(4)			100		ns
VCM_DIAG$_{POS}$	Positve Diagnostic pulse amplitude(4)	Base pulse = VCM; High level pulse = VCM+5%VREF		165		mV
VCM_DIAG$_{NEG}$	Negative Diagnostic pulse amplitude(4)	Base pulse = VCM; High level pulse = VCM-5%VREF		165		mV
VCM_DIAG_acc	Diagnostics Pulse accuracy(4)			0.1		%
VCM_DIAG$_{tR}$	Diagnostics Pulse rise time(4)	10% to 90%, C = 15pF		10		us
VCM_DIAG$_{tF}$	Diagnostics Pulse fall time(4)	90% to 10%, C=15pF		10		us

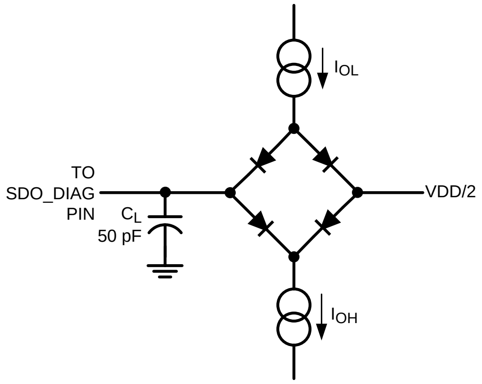
(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that TJ = TA. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where TJ >TA.

(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using the Statistical Quality Control (SQC) method.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.

(4) This parameter is specified by design and/or characterization and is not tested in production.

Test Circuit Diagrams



TEST CIRCUIT DIAGRAMS

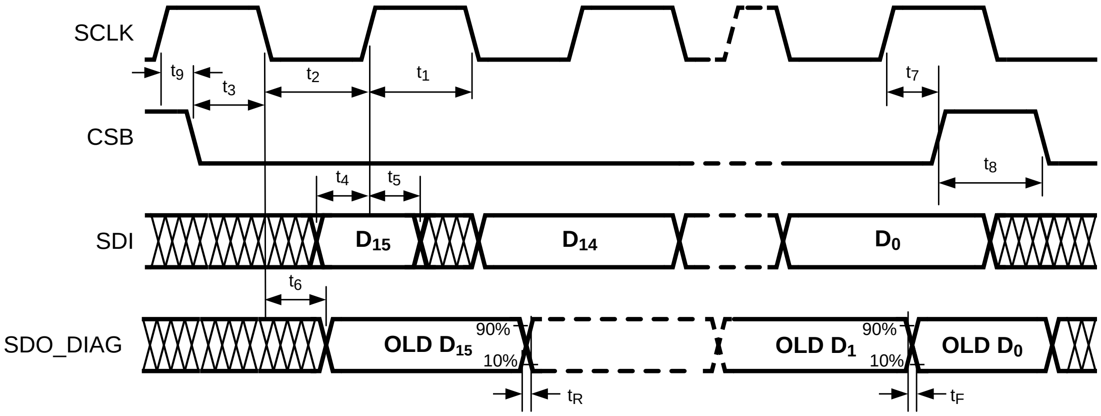


Figure 2. SERIAL INTERFACE TIMING DIAGRAM

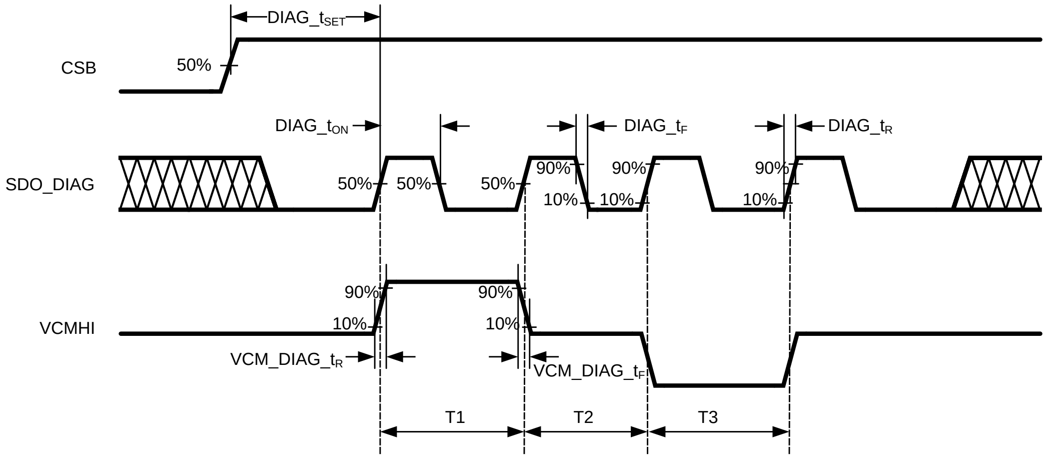


Figure 3. DIAGNOSTIC TIMING DIAGRAM

Typical Performance Characteristics

Unless otherwise specified, T_A=25°C, V_S=(VDD-GND)=3.3V, VREF=3.3V.

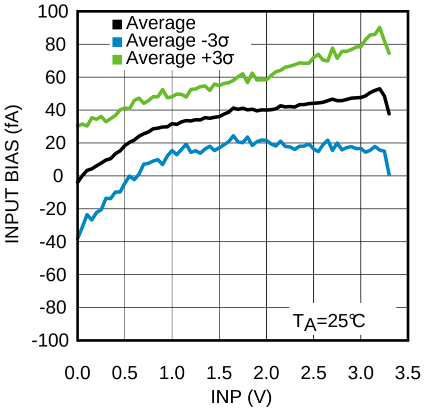

pH Buffer Input Bias Current vs. V_{INP} - Device ON

Figure 4.

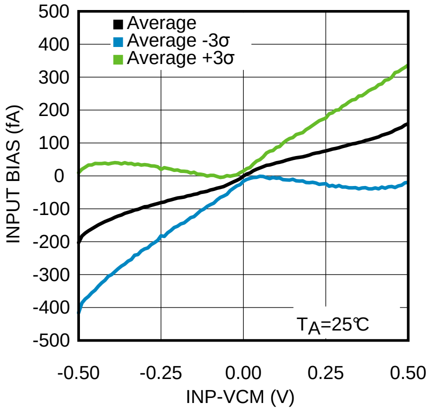

pH Buffer Input Bias Current vs. V_{INP} - Device OFF

Figure 5.

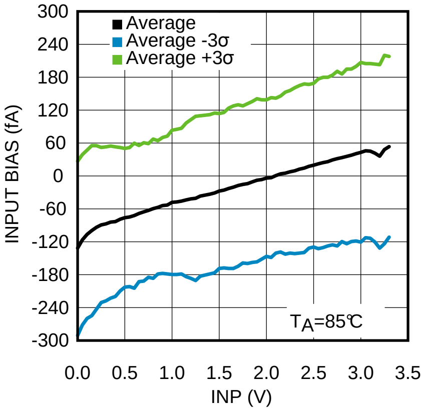

pH Buffer Input Bias Current vs. V_{INP} - Device ON

Figure 6.

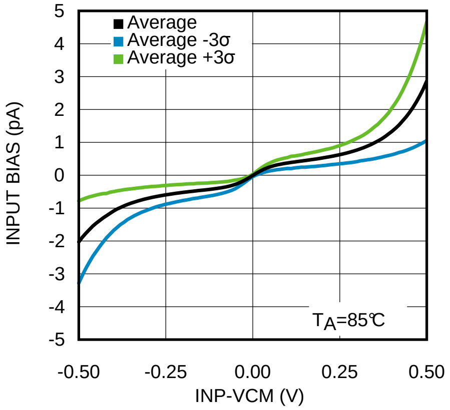

pH Buffer Input Bias Current vs. V_{INP} - Device OFF

Figure 7.

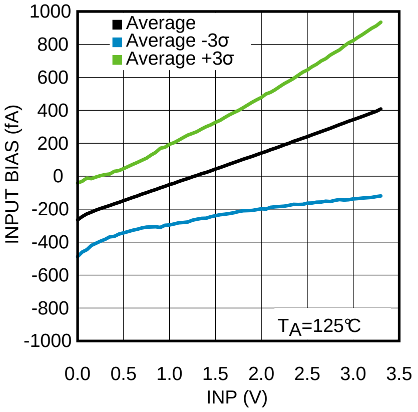

pH Buffer Input Bias Current vs. V_{INP} - Device ON

Figure 8.

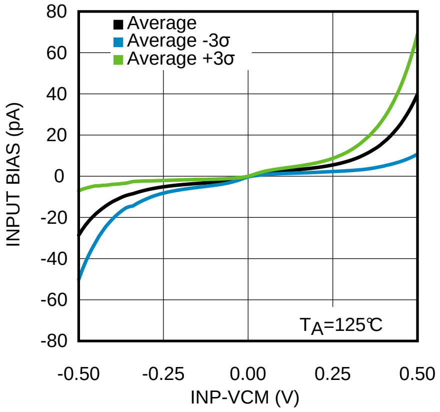
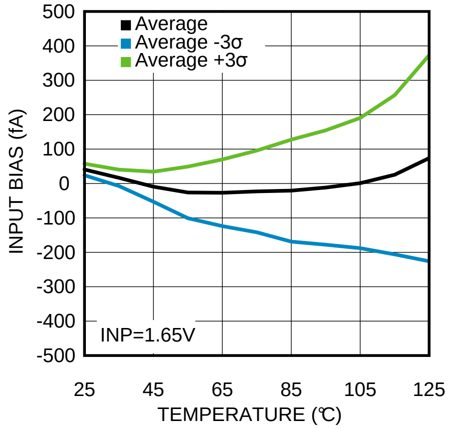

pH Buffer Input Bias Current vs. V_{INP} - Device OFF

Figure 9.

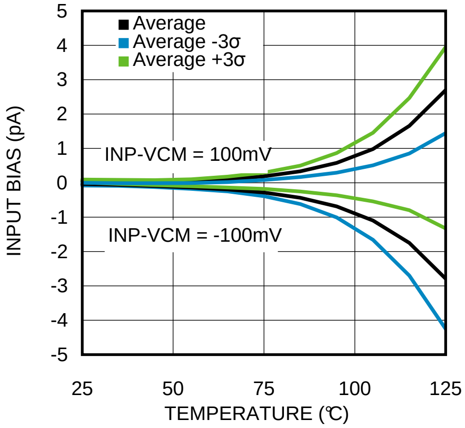
Typical Performance Characteristics (continued)

Unless otherwise specified, T_A=25°C, V_S=(VDD-GND)=3.3V, VREF=3.3V.



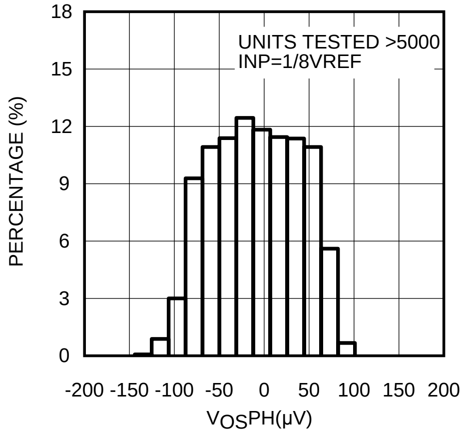
pH Buffer Input Bias Current vs. Temp - Device ON

Figure 10.



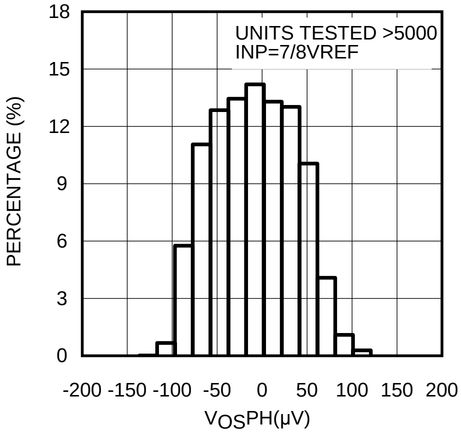
pH Buffer Input Bias Current vs. Temp - Device OFF

Figure 11.



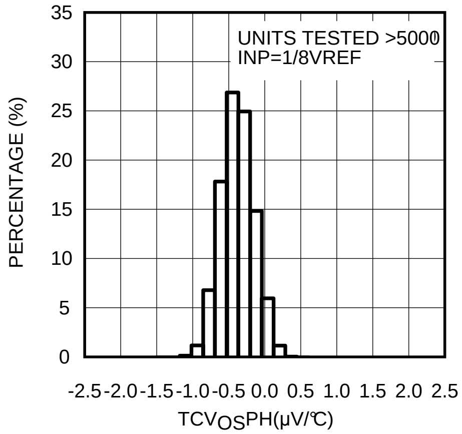
pH Buffer Input Voltage Offset

Figure 12.



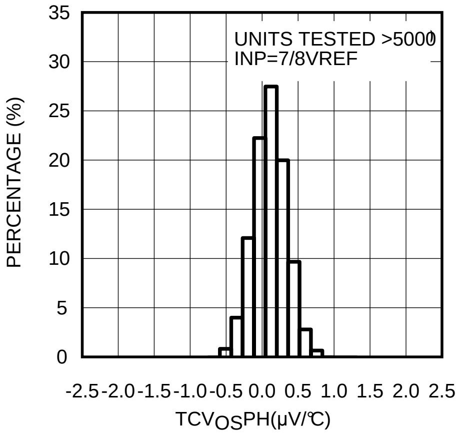
pH Buffer Input Voltage Offset

Figure 13.



pH Buffer TcVos

Figure 14.



pH Buffer TcVos

Figure 15.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A=25°C, V_S=(VDD-GND)=3.3V, VREF=3.3V.

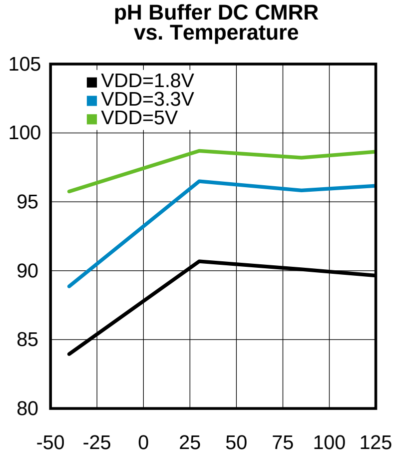


Figure 16.

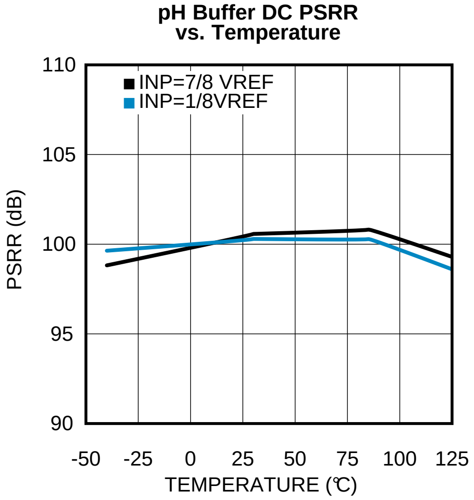


Figure 17.

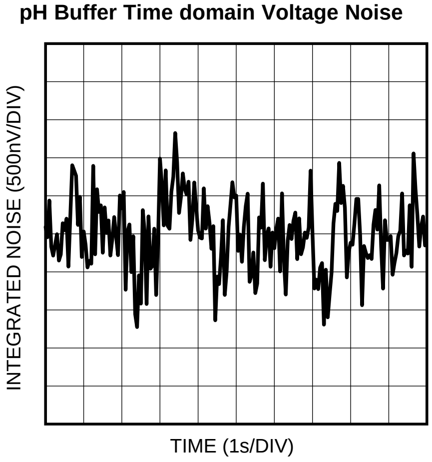


Figure 18.

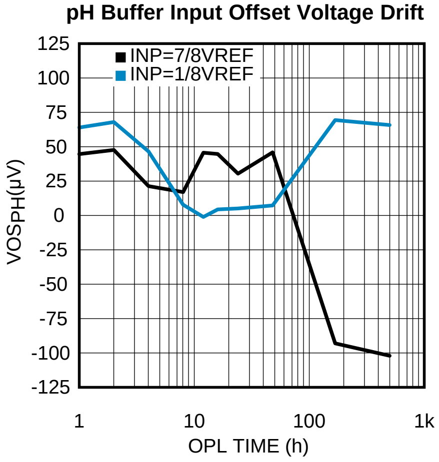


Figure 19.

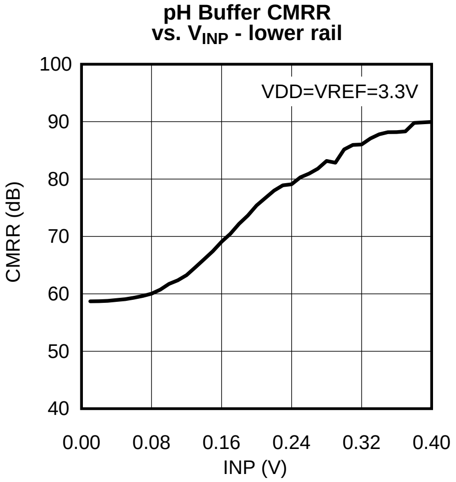


Figure 20.

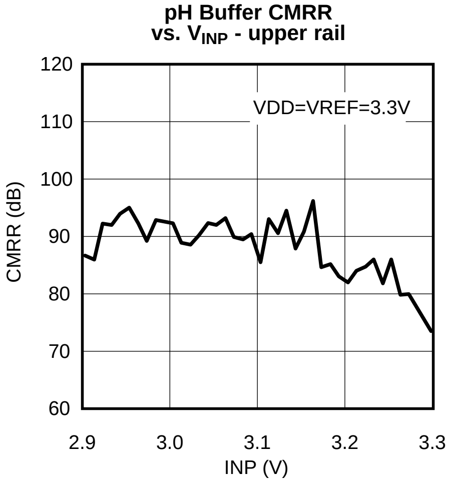


Figure 21.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A=25°C, V_S=(VDD-GND)=3.3V, VREF=3.3V.

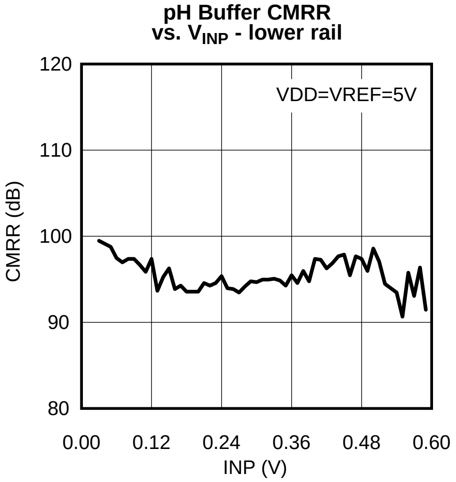


Figure 22.

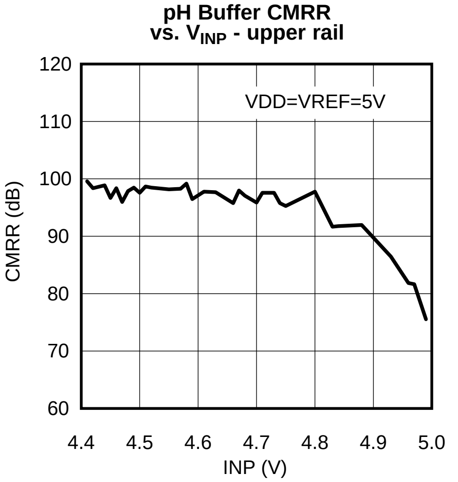


Figure 23.

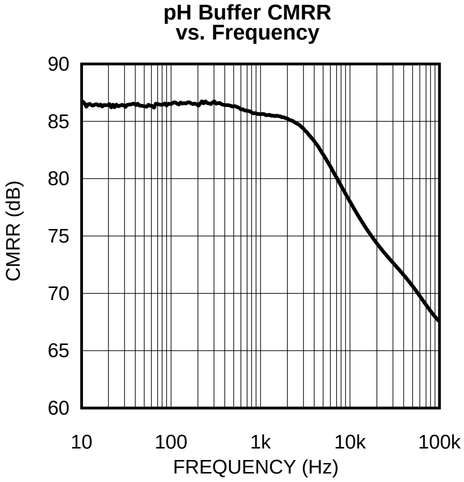


Figure 24.

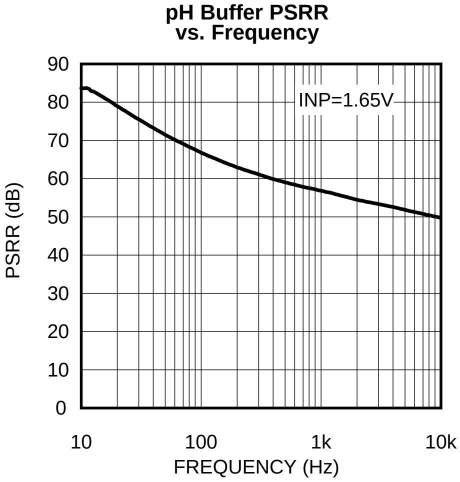


Figure 25.

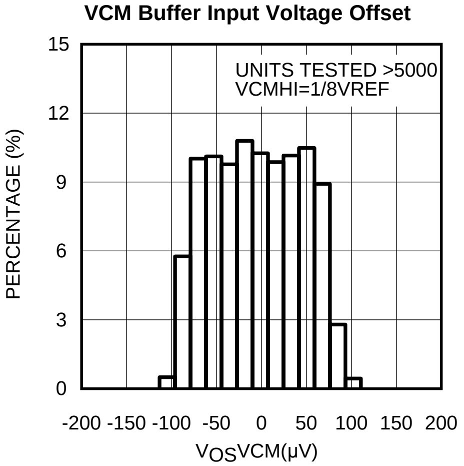


Figure 26.

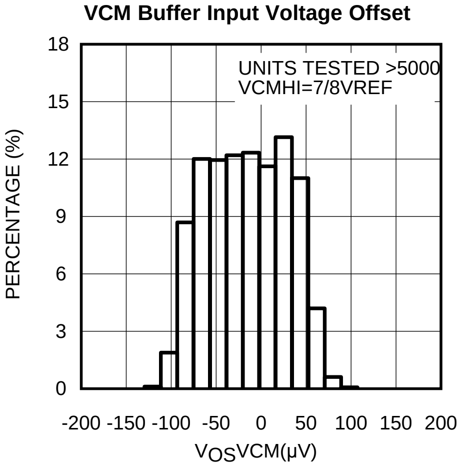


Figure 27.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A=25°C, V_S=(VDD-GND)=3.3V, VREF=3.3V.

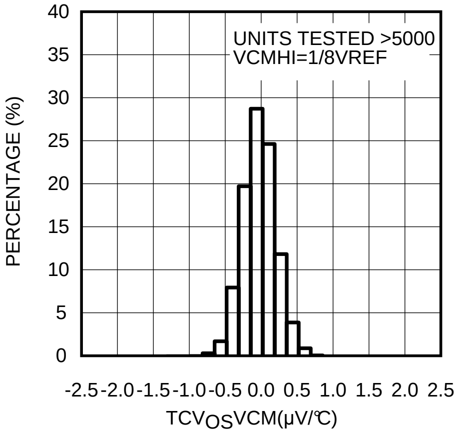

VCM Buffer TcVos

Figure 28.

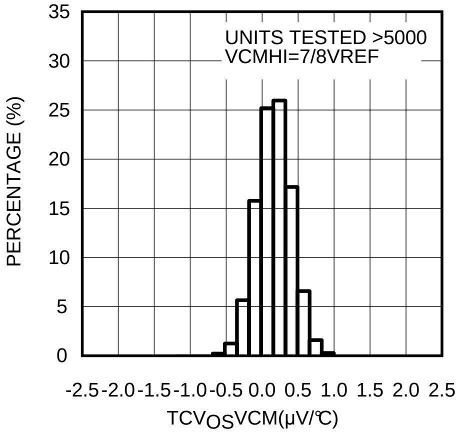

VCM Buffer TcVos

Figure 29.

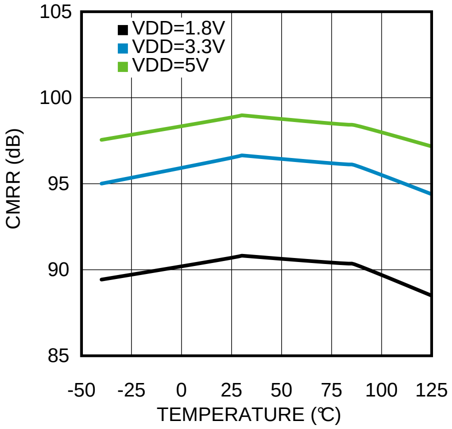

VCM Buffer DC CMRR vs. Temperature

Figure 30.

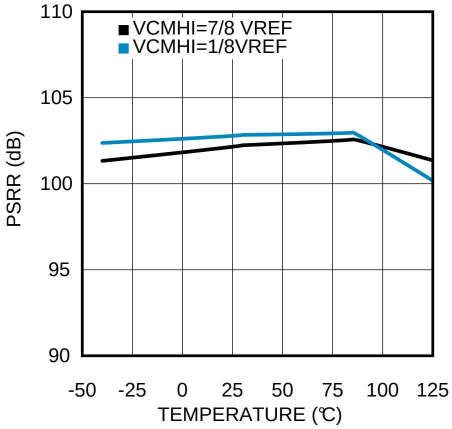

VCM Buffer DC PSRR vs. Temperature

Figure 31.

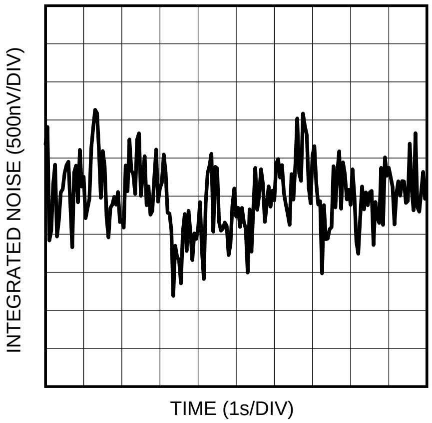

VCM Buffer Time domain Voltage Noise

Figure 32.

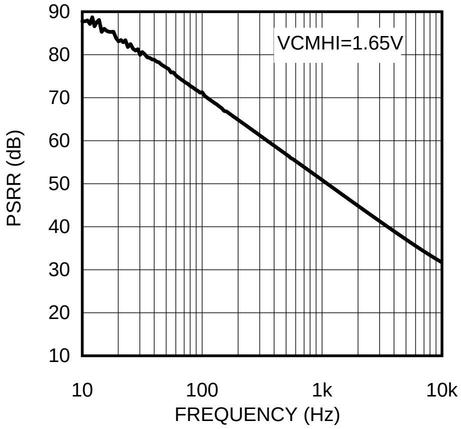
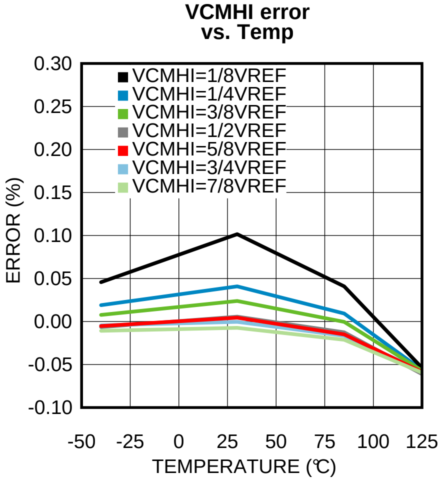

VCM Buffer PSRR vs. Frequency

Figure 33.

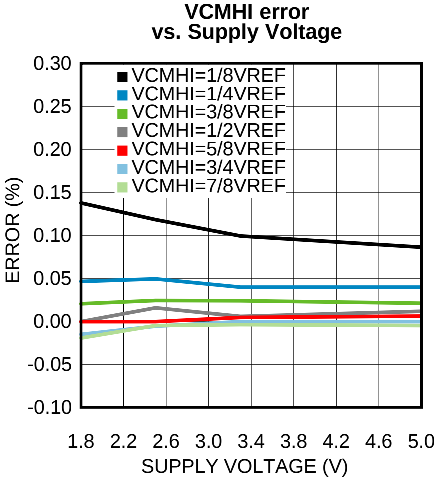
Typical Performance Characteristics (continued)

Unless otherwise specified, T_A=25°C, V_S=(VDD-GND)=3.3V, VREF=3.3V.



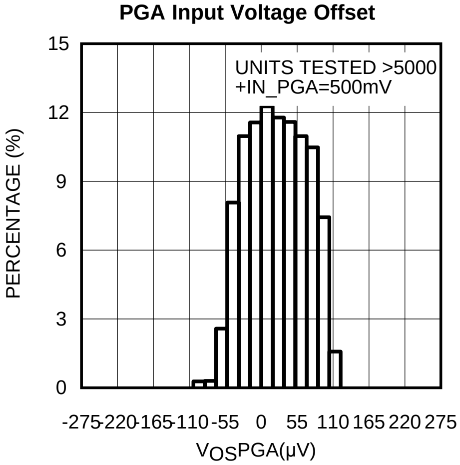
VCMHI error vs. Temp

Figure 34.



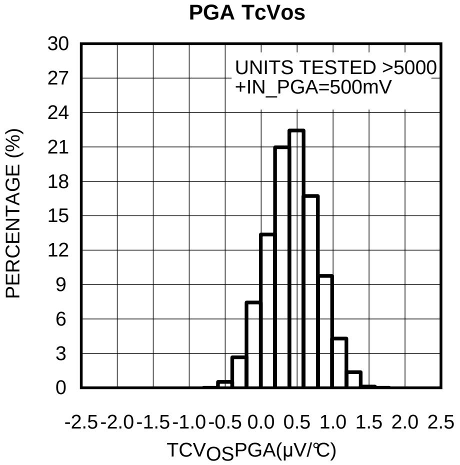
VCMHI error vs. Supply Voltage

Figure 35.



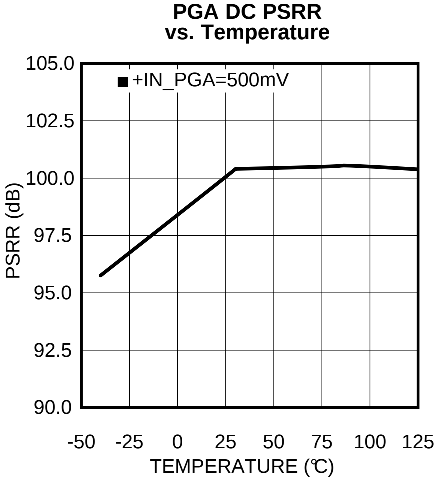
PGA Input Voltage Offset

Figure 36.



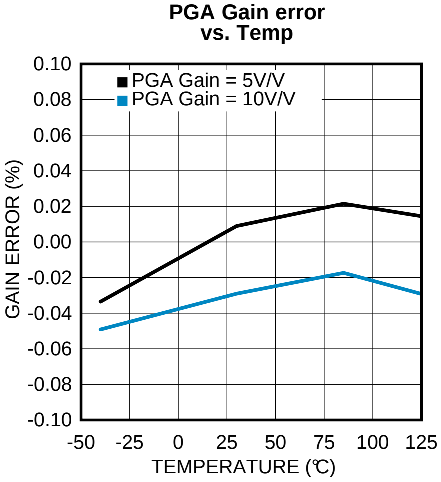
PGA TcVos

Figure 37.



PGA DC PSRR vs. Temperature

Figure 38.



PGA Gain error vs. Temp

Figure 39.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A=25°C, V_S=(VDD-GND)=3.3V, VREF=3.3V.

PGA Time domain Voltage Noise

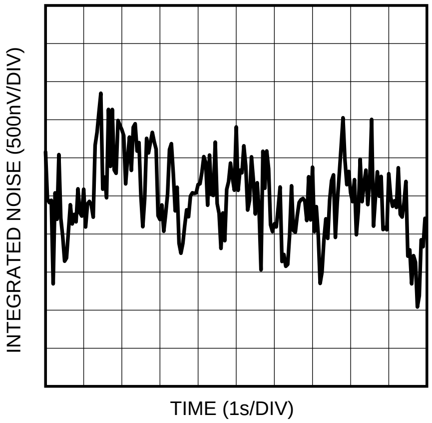


Figure 40.

PGA PSRR vs. Frequency

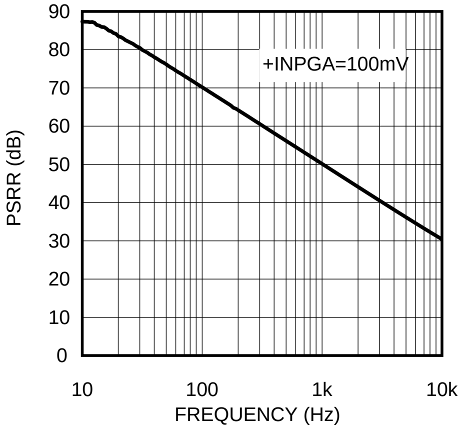


Figure 41.

Current Source (I_{cs}=100µA)

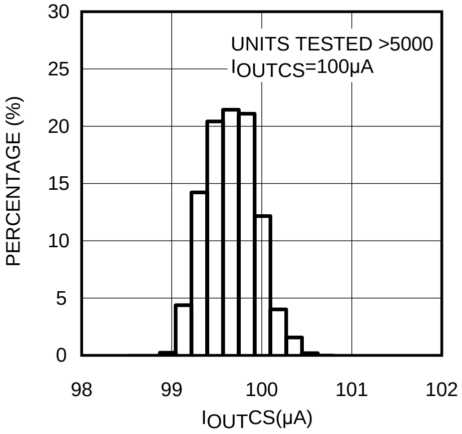


Figure 42.

Temperature coefficient Current Source (I_{cs}=100µA)

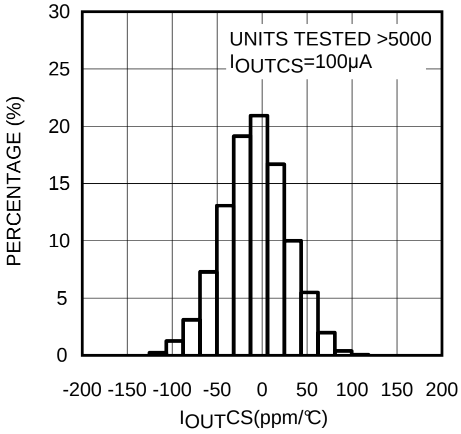


Figure 43. g

Current Source (I_{cs}=200µA)

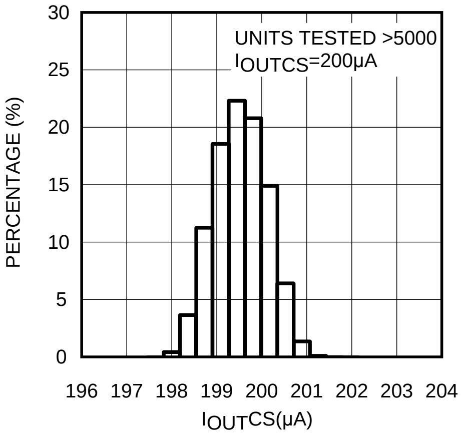


Figure 44.

Temperature coefficient Current Source (I_{cs}=200µA)

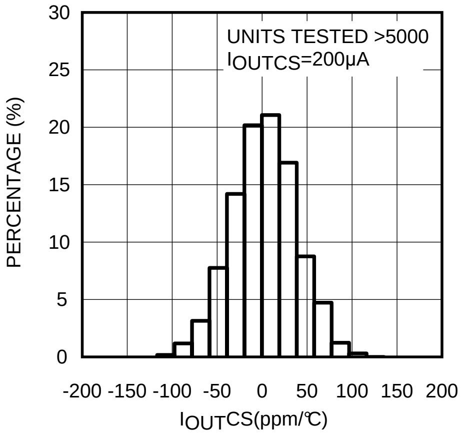
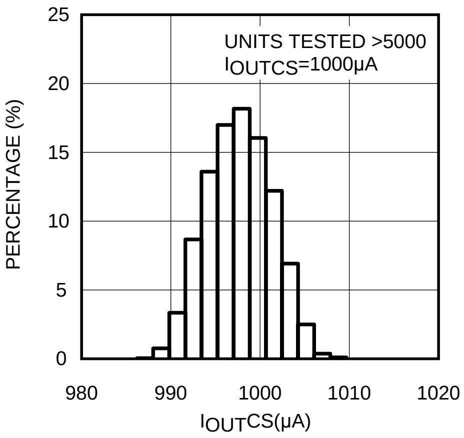


Figure 45.

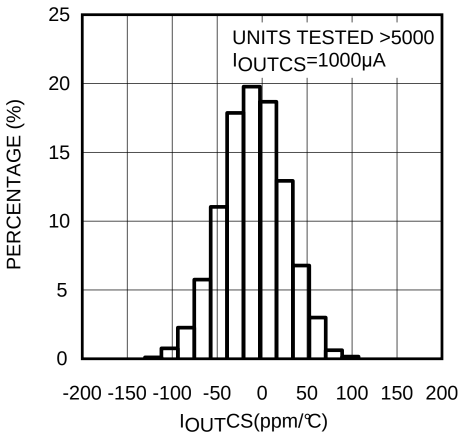
Typical Performance Characteristics (continued)

Unless otherwise specified, T_A=25°C, V_S=(VDD-GND)=3.3V, VREF=3.3V.



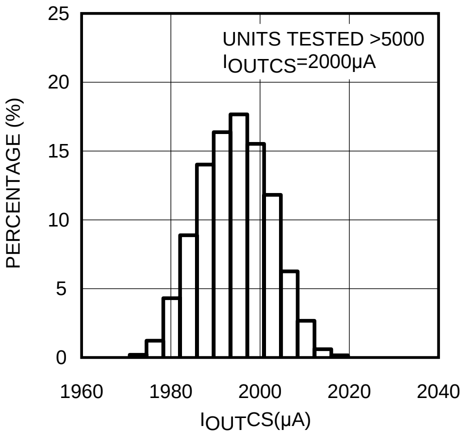
Current Source (I_{cs}=1000µA)

Figure 46.



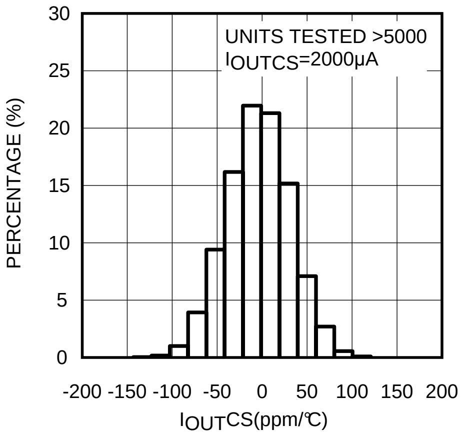
Temperature coefficient Current Source (I_{cs}=1000µA)

Figure 47.



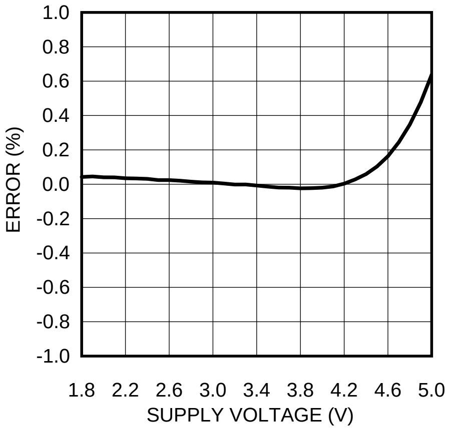
Current Source (I_{cs}=2000µA)

Figure 48.



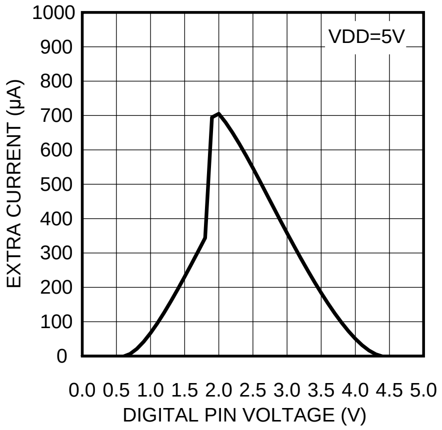
Temperature coefficient Current Source (I_{cs}=2000µA)

Figure 49.



Current Source accuracy (I_acc$_{CS}$) vs. Supply Voltage

Figure 50.



Supply current vs. digital input voltage

Figure 51.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A=25°C, V_S=(VDD-GND)=3.3V, VREF=3.3V.

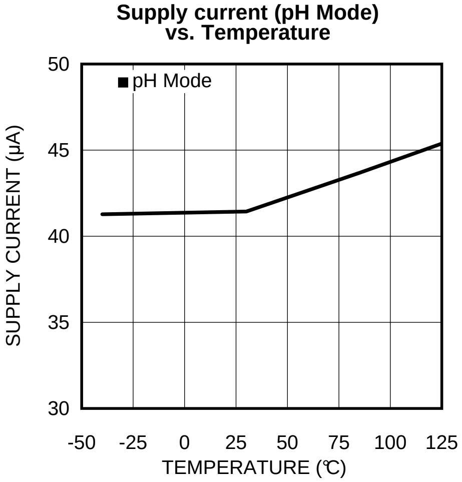


Figure 52.

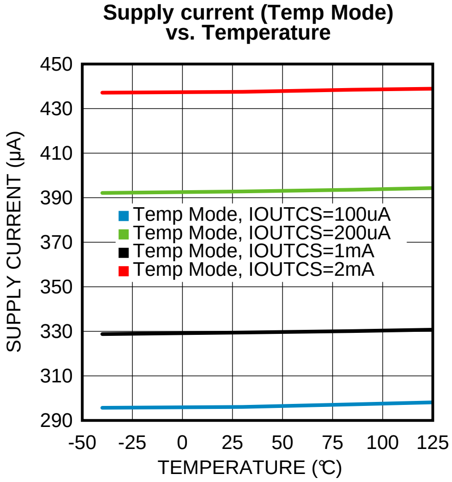


Figure 53.

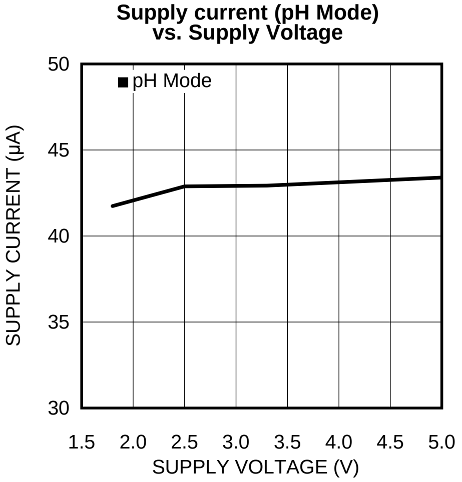


Figure 54.

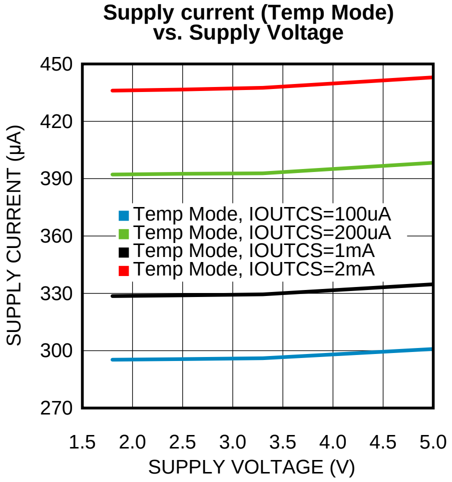


Figure 55.

FUNCTIONAL DESCRIPTION

GENERAL INFORMATION

The LMP91200 is a configurable sensor AFE for use in low power analytical sensing applications. The LMP91200 is designed for 2-electrode sensors. This device provides all of the functionality needed to detect changes based on a delta voltage at the sensor. Optimized for low-power applications, the LMP91200 works over a voltage range of 1.8V to 5.5V. With its extremely low input bias current it is optimized for use with pH sensors. Also in absence of supply voltage the very low input bias current reduces degradation of the pH probe when connected to the LMP91200. The Common Mode Output pin (VOCM) provides a common mode offset, which can be programmed to different values to accommodate pH sensor output ranges. For applications requiring a high impedance common mode this option is also available. Two guard pins provide support for high parasitic impedance wiring. Support for an external Pt1000, Pt100, or similar temperature sensor is integrated in the LMP91200. The control of this feature is available through the SPI interface. Additionally, a user controlled sensor diagnostic test is available. This function tests the sensor for proper connection and functionality.

pH Buffer

The pH Buffer is a unity gain buffer with a input bias current in the range of tens fA at room. Its very low bias current introduces a negligible error in the measurement of the pH. The ph buffer is provided with 2 guard pins (GUARD1, GUARD2) in order to minimize the leakage of the input current and to make easy the design of a guard ring.

Common mode selector and VCM buffer

The common mode selector allows to set 7 different values of common mode voltage (from 1/8 VREF to 7/8VREF with 1/8 VREF step) according to the applied voltage reference at VREF pin. Both buffered and unbuffered version of the set common mode voltage are available respectively at VCM pin and VCMHI pin. A copy of the buffered version is present at VOCM pin in case of differential measurement.

Current Source and PGA

The internal current source is programmable current generator which is able to source 4 different current values (100µA, 200µA, 1mA, 2mA) in order to well stimulate Pt100 and Pt1000 thermal resistor. The selected current is sourced from either RTD pin (pin for thermal resistor connection) or CAL pin (pin for reference resistor connection). The voltage across either the thermal resistor or the reference resistor is amplified by the PGA (5V/V, 10V/V) and provided at the VOUT pin when the LMP91200 is set in Temperature measurement mode.

Output Muxes

The output of the LMP91200 can be configured to support both differential and single ended ADC's. When measuring pH the Output signal can be referred either to VCM or GND. When measuring temperature the Output signal is referred to GND. The Output configuration is controlled through the SPI interface.

SERIAL CONTROL INTERFACE OPERATION

All the features of the LMP91200 (Mode of Operation, PGA Gain, Voltage reference, Diagnostic) are by data stored in a programming register. Data to be written into the control register is first loaded into the LMP91200 via the serial interface. The serial interface employs a 16-bit shift register. Data is loaded through the serial data input, SDI. Data passing through the shift register is output through the serial data output, SDO_DIAG. The serial clock, SCK controls the serial loading process. All sixteen data bits are required to correctly program the LMP91200. The falling edge of CSB enables the shift register to receive data. The SCK signal must be high during the falling and rising edge of CSB. Each data bit is clocked into the shift register on the rising edge of SCLK. Data is transferred from the shift register to the holding register on the rising edge of CSB.

Configuration Register

Bit	Name	Description
D15	MEAS_MODE	**0 pH measurement (default)** 1 Temp measurement
D14	I_MUX	**0 RTD (default)** 1 CAL
[D13:D12]	I_VALUE	**00 100µA (default)** 01 200 µA 10 1 mA 11 2 mA
D11	PGA	**0 5 V/V (default)** 1 10 V/V
[D10 :D8]	VCM	011 7/8Vref 010 3/4Vref 001 5/8Vref **000 1/2Vref (default)** 100 1/2Vref 101 3/8Vref 110 1/4Vref 111 1/8 Vref
D7	VOCM	**0 VOCM (default)** 1 GND
D6	DIAG_EN	**0 DIAG pin disabled (default)** 1 DIAG pin enabled
[D5 :D0]	RESERVED	RESERVED

Application Information

Theory of pH measurement

pH electrode measurements are made by comparing the readings in a sample with the readings in standards whose pH has been defined (buffers). When a pH sensing electrode comes in contact with a sample, a potential develops across the sensing membrane surface and that membrane potential varies with pH. A reference electrode provides a second, unvarying potential to quantitatively compare the changes of the sensing membrane potential. Nowadays pH electrodes are composed of a sensing electrode with the reference electrode built into the same electrode body, they are called combination electrodes. A high input impedance meter serves as the readout device and calculates the difference between the reference electrode and sensing electrode potentials in millivolts. The millivolts are then converted to pH units according to the Nernst equation.

Electrode behavior is described by the Nernst equation:

E = Eo + (2.3 RT/nF) log aH+, where

E is the measured potential from the sensing electrode,

Eo is related to the potential of the reference electrode,

(2.3 RT/nF) is the Nernst factor,

log aH+ is the pH, (aH+ = activity of Hydrogen ions).

2.3 RT/nF, includes the Gas Law constant (R), Faraday’s constant (F), the temperature in degrees Kelvin (T) and the stoichiometric number of ions involved in the process (n). For pH, where n = 1, the Nernst factor is 2.3 RT/F. Since R and F are constants, the factor and therefore electrode behavior is dependent on temperature. The Nernst Factor is equivalent to the electrode slope which is a measure of the electrode response to the ion being detected. When the temperature is 25 °C, the theoretical Nernst slope is 59.16 mV/pH unit.

LMP91200 in pH meter with ATC (Automatic Temperature Compensation)

The most common cause of error in pH measurements is temperature. Temperature variations can influence pH for the following reasons:

- the electrode slope will change with variations in temperature
- buffer and sample pH values will change with temperature

Measurement drift can occur when the internal elements of the pH and reference electrodes are reaching thermal equilibrium after a temperature change. When the pH electrode and temperature probe are placed into a sample that varies significantly in temperature, the measurements can drift because the temperature response of the pH electrode and temperature probe may not be similar and the sample may not have a uniform temperature, so the pH electrode and temperature probe are responding to different environments.

The pH values of buffers and samples will change with variations in temperature because of their temperature dependent chemical equilibria. The pH electrode should be calibrated with buffers that have known pH values at different temperatures. Since pH meters are unable to correct sample pH values to a reference temperature, due to the unique pH versus temperature relationship of each sample, the calibration and measurements should be performed at the same temperature and sample pH values should be recorded with the sample temperature.

The LMP91200 offers in one package all the features to build a pH meter with ATC. Through the SPI Interface is possible to switch from pH measurement mode to temperature measurement mode and collect both temperature and potential of sensing electrode.

pH measurement

The output of a pH electrode ranges from 415 mV to −415 mV as the pH changes from 0 to 14 at 25°C. The output impedance of a pH electrode is extremely high, ranging from 10 MΩ to 1000 MΩ. The low input bias current of the LMP91200 allows the voltage error produced by the input bias current and electrode resistance to be minimal. For example, the output impedance of the pH electrode used is 10 MΩ, if an op amp with 3 nA of Ibias is used, the error caused due to this amplifier’s input bias current and the source resistance of the pH electrode is 30 mV! This error can be greatly reduced to 1.25µV by using the LMP91200.

The pH measurement with the LMP91200 is straightforward, the pH electrode needs to be connected between VCM pin and INP pin. The voltage at VCM pin represent the internal zero of the system, so the potential of the electrode (voltage at INP pin) will be refered to VCM voltage. The common mode voltage can be set to well fit the input dynamic range of an external ADC connected between VOUT and VOCM when the LMP91200 is configured with differential output. In Table 1 a typical configuration of the register of the LMP91200 with VCM set at 1/2 of VREF and differential output.

Table 1. Configuration register: pH measurement

Bit	Name	Description
D15	MEAS_MODE	0 pH measurement
D14	I_MUX	Leave these bits as they have been configured for the temperature measurement.
[D13:D12]	I_VALUE	
D11	PGA	
[D10 :D8]	VCM	000 1/2 VREEF
D7	VOCM	0 VOCM
D6	DIAG_EN	0 DIAGNOSTIC disabled
[D5 :D0]	RESERVED	RESERVED

Temperature measurement

The LMP91200 supports temperature measurement with RTD like Pt100 and Pt1000. According to the RTD connected to the LMP91200 the right amount of exciting current can be programmed: 100µA for Pt1000 and 1mA for Pt100, resulting in a nominal voltage drop of 100mV for both RTD's at 0°C. This voltage can be amplified, using an internal amplifier with a factor of 5 or 10 V/V. In case of high precision temperature measurement it is possible to connect an external high accuracy resistor and implement a calibration procedure. The exciting current sourced by the LMP91200 can be multiplexed either into the RTD or into the external precision resistor in order to implement a 2-step or 3-step temperature measurement. The multi step temperature measurements allows to remove uncertainty of the temperature signal path.

1-step measurement

In the one step measurement the voltage across the RTD (Pt100, Pt1000) due to the exciting current is amplified and measured. The temperature can be calculated according to the following equation:

$$\textbf{Temp(°C) = (Pt}_{\textbf{RES\_}}\textbf{calculated – Pt}_{\textbf{RES\_}}\textbf{nominal)/alpha}$$

where

- **alpha** is the thermal coefficient of the RTD (it depends on the selected Ptres)
- **Pt$_{RES_}$nominal** is the value of the Ptres at 0degC (1)

$$\textbf{Pt}_{\textbf{RES\_}}\textbf{calculated = (VOUT\_Pt}_{\textbf{RES}}\textbf{/I\_Pt)/PGA\_GAIN}$$

where

- **VOUT_Pt$_{RES}$** is the amplified voltage across the RTD at VOUT pin (ground referred) when the LMP91200 is configured according to Table 2
- **I_Pt** is the value of the selected exciting current according to the RTD
- **PGA_GAIN** is the selected gain of the PGA (2)

Inserting Equation 2 in Equation 1 the temperature is given by the following equation:

$$\textbf{Temp(°C) = Temp(°C) = ((VOUT\_Pt}_{\textbf{RES}}\textbf{/I\_Pt)/PGA\_GAIN – Pt}_{\textbf{RES\_}}\textbf{nominal)/alpha} \tag{3}$$

Table 2. Configuration register: 1-step measurement

Bit	Name	Description
D15	MEAS_MODE	1 Temp measurement
D14	I_MUX	0 RTD
[D13:D12]	I_VALUE	00 100µA (Pt1000) 10 1 mA (Pt100)
D11	PGA	1 10 V/V
[D10 :D8]	VCM	Leave these bits as they have been configured for the pH measurement.
D7	VOCM	1 GND
D6	DIAG_EN	0 DIAGNOSTIC disabled
[D5 :D0]	RESERVED	RESERVED

The 1-step temperature measurement has a precision of about ±3°C.

2-step measurement

This method requires 2 acquisitions and a precision resistor (R_{REF}) connected between CAL and GND pin, (the RTD is always connected between RTD and GND pin). The first acquisitions measure the voltage across the precision resistor in the same condition (source current and PGA gain) of the next temperature measurement in order to remove the uncertainty on the current source value. The second acquisition measures the voltage across the RTD (similar to the 1-step measure), in this case the formula to calculate the temperature is a little bit more complicate in order to take in account the non-ideality of the system (source current error).

$$\mathbf{Temp(°C) = (Pt_{RES}\_calculated – Pt_{RES}\_nominal) /alpha}$$

where

- **alpha** is the thermal coefficient of the RTD (it depends on the selected Ptres)
- **Ptres_nominal** is the value of the Ptres at 0degC (4)

$$\mathbf{Pt_{RES}\_calculated=(VOUT\_Pt_{RES}/PGA\_GAIN)/I\_true}$$

where

- **VOUT_Pt$_{RES}$** is the amplified voltage across the RTD at VOUT pin (ground referred), when the LMP91200 is configured according to Table 4
- **I_true** is the real current which alternatively flows in the external precison resistance R_{REF} and in the RTD
- **PGA_GAIN** is the selected gain of the PGA (5)

$$\mathbf{I\_true=(VOUT\_R_{REF})/(PGA\_GAIN{*}R_{REF})}$$

where

- **VOUT_R$_{REF}$** is the amplified voltage across the R_{REF} at VOUT pin (ground referred), when the LMP91200 is configured according to Table 3 (6)

Inserting Equation 5 and Equation 6 in Equation 4 the temperature is given by the following equation:

$$\mathbf{Temp(°C) = ((VOUT\_Pt_{RES} /VOUT\_R_{REF}){*}R_{REF}– Pt_{RES}\_nominal) /alpha} \quad (7)$$

Table 3.

Bit	Name	Description
D15	MEAS_MODE	1 Temp measurement
D14	I_MUX	1 RCAL
[D13:D12]	I_VALUE	00 100µA (Pt1000) 10 1 mA (Pt100)
D11	PGA	1 10 V/V
[D10 :D8]	VCM	Leave these bits as they have been configured for the pH measurement.
D7	VOCM	1 GND
D6	DIAG_EN	0 DIAGNOSTIC disabled
[D5 :D0]	RESERVED	RESERVED

Table 4. Configuration register: 2-step measurement

Bit	Name	Description
D15	MEAS_MODE	1 Temp measurement
D14	I_MUX	0 RTD
[D13:D12]	I_VALUE	00 100µA (Pt1000) 10 1 mA (Pt100)
D11	PGA	1 10 V/V
[D10 :D8]	VCM	Leave these bits as they have been configured for the pH measurement.
D7	VOCM	1 GND
D6	DIAG_EN	0 DIAGNOSTIC disabled
[D5 :D0]	RESERVED	RESERVED

The 2-step temperature measurement has a precision of about ±0.3°C (with R_{REF} @ 0.01% of tolerance) which is good enough in most of pH meter applications.

3-step measurement

This method requires 3 acquisitions and a precision resistor (R_{REF}) connected between CAL and GND pin, (the RTD is always connected between RTD and GND pin). The first two acquisitions measure the voltage across the precision resistor in 2 different conditions (2 different exciting current and 2 PGA gains) in order to remove the uncertainty of the current source value and the offset of the path. The third acquisition measures the voltage across the RTD (similar to the 1-step measure), in this case the formula to calculate the temperature is more complicate in order to take in account the non-ideality of the system (offset, source current error).

$$\text{Temp(°C)} = (Pt_{RES\_}\text{calculated} - Pt_{RES\_}\text{nominal}) / \text{alpha}$$

where

- **alpha** is the thermal coefficient of the RTD (it depends on the selected Ptres)
- **Ptres_nominal** is the value of the Ptres at 0degC (8)

$$Pt_{RES\_}\text{calculated} = ((\text{VOUT\_}Pt_{RES}/\text{PGA\_GAIN}) - \text{Vos}) / \text{I\_true}$$

where

- **VOUT_Pt_{RES}** is the amplified voltage across the RTD at VOUT pin (ground referred), when the LMP91200 is configured according to Table 7
- **I_true** is the real current which alternatively flows in the external precison resistance R_{REF} and in the RTD
- **PGA_GAIN** is the selected gain of the PGA
- **Vos** is the offset of the path (9)

$$\mathbf{Vos=(VOUT\_R_{REF0}-VOUT\_R_{REF1})/5}$$

where

- **VOUT_R_{REF0}** is the amplified voltage across the R_{REF} at VOUT pin (ground referred), when the LMP91200 is configured according to Table 5
- **VOUT_$R_{REF\ 1}$**is the amplified voltage across the R_{REF} at VOUT pin (ground referred), when the LMP91200 is configured according to Table 6 (10)

$$\mathbf{I\_true=(2*VOUT\_R_{REF1}-VOUT\_R_{REF0})/(10*R_{REF})} \quad (11)$$

Inserting Equation 9, Equation 10 and Equation 11 in Equation 8 the temperature is given by the following equation:

$$\mathbf{Temp(°C) = (((VOUT\_Pt_{RES}/PGA\_GAIN)-(VOUT\_R_{REF0}-VOUT\_R_{REF1})/5)/((2*VOUT\_R_{REF1}-VOUT\_R_{REF0})/(10*R_{REF}))–Pt_{RES}\_nominal)\ /alpha} \quad (12)$$

Table 5.

Bit	Name	Description
D15	MEAS_MODE	1 Temp measurement
D14	I_MUX	1 RCAL
[D13:D12]	I_VALUE	01 200µA (Pt1000) 11 2 mA (Pt100)
D11	PGA	0 5 V/V
[D10 :D8]	VCM	Leave these bits as they have been configured for the pH measurement.
D7	VOCM	1 GND
D6	DIAG_EN	0 DIAGNOSTIC disabled
[D5 :D0]	RESERVED	RESERVED

Table 6.

Bit	Name	Description
D15	MEAS_MODE	1 Temp measurement
D14	I_MUX	1 RCAL
[D13:D12]	I_VALUE	00 100µA (Pt1000) 10 1 mA (Pt100)
D11	PGA	1 10 V/V
[D10 :D8]	VCM	Leave these bits as they have been configured for the pH measurement.
D7	VOCM	1 GND
D6	DIAG_EN	0 DIAGNOSTIC disabled
[D5 :D0]	RESERVED	RESERVED

Table 7. Configuration register: 3-step measurement

Bit	Name	Description
D15	MEAS_MODE	1 Temp measurement
D14	I_MUX	0 RTD
[D13:D12]	I_VALUE	00 100µA (Pt1000) 10 1 mA (Pt100)
D11	PGA	1 10 V/V
[D10 :D8]	VCM	Leave these bits as they have been configured for the pH measurement.
D7	VOCM	1 GND
D6	DIAG_EN	0 DIAGNOSTIC disabled
[D5 :D0]	RESERVED	RESERVED

The 3-step temperature measurement can reach a precision as high as ±0.1°C (with R_{REF} @ 0.01% of tolerance) when the analog signal is acquired by at least 16 bit ADC. With lower number of bit ADC this method gives the same result of the 2-step measurement due to the low voltage offset of the signal path. As rule of thumb, the 3-step temperature measurement gives good result if he the LSB of the ADC is less than the input offset of the PGA.

Diagnostic Feature

The diagnostic function allows detecting the presence of the sensor and checking the connection of the sensor. A further analysis of the answer of the pH probe to the diagnostic stimulus allows estimating the aging of the pH probe. With the diagnostic function is possible to change slightly (+/- 5% VREF) the Common mode voltage. If the sensor is present it reacts, this reaction gives some information on the status of the connection, the presence of the sensor and its aging. In fact a typical symptom of the aging of a pH probe is the slowness in the answer. It means that a pH probe answers with a smoother step to the diagnostic stimulus as its age increases.

The procedure is enabled and disabled by SPI (refer to). Until bit D6 is at low logic level, VCM stays at the programmed voltage independently by the SDO_DIAG pin status. When bit D6 is tied at high logic level, on the first rising edge of SDO_DIAG, a positive pulse is generate. At the second positive rising edge of SDO_DIAG pin, the positive pulse ends. At the third positive rising edge of SDO_DIAG a negative pulse is generated. At the forth positive rising edge of the SDO_DIAG the negative pulse ends and the routine is stopped and cannot restart until bit D6 is set again at 1.

Layout Consideration

In pH measurement, due to the high impedance of the ph Electrode, careful circuit layout and assembly are required. Guarding techniques are highly recommended to reduce parasitic leakage current by isolating the LMP91200's input from large voltage gradients across the PC board. A guard is a low impedance conductor that surrounds an input line and its potential is raised to the input line's voltage. The input pin should be fully guarded as shown in Figure 56. The guard traces should completely encircle the input connections. In addition, they should be located on both sides of the PCB and be connected together. The LMP91200 makes the guard ring easy to be implemented without any other external op amp. The ring needs to be connected to the guard pins (GUARD1 and GUARD2) which are at the same potential of the INP pin. Solder mask should not cover the input and the guard area including guard traces on either side of the PCB. Sockets are not recommended as they can be a significant leakage source. After assembly, a thorough cleaning using commercial solvent is necessary.

In Figure 56 is showed a typical guard ring circuit when the LMP912000 is interfaced to a pH probe trough a triaxial cable/connector, usually known as 'TRIAX'. The signal conductor and the guard of the triax should be kept at the same potential; therefore, the leakage current between them is practically zero. Since triax has an extra layer of insulation and a second conducting sheath, it offers greater rejection of interference than coaxial cable/connector.

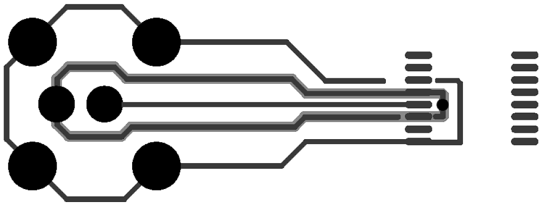


Figure 56. Circuit Board Guard Layout

REVISION HISTORY

Changes from Revision B (March 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	25

PACKAGE OPTION ADDENDUM

22-Mar-2013

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMP91200MT/NOPB	ACTIVE	TSSOP	PW	16	92	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR		LMP912 00MT	Samples
LMP91200MTX/NOPB	ACTIVE	TSSOP	PW	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR		LMP912 00MT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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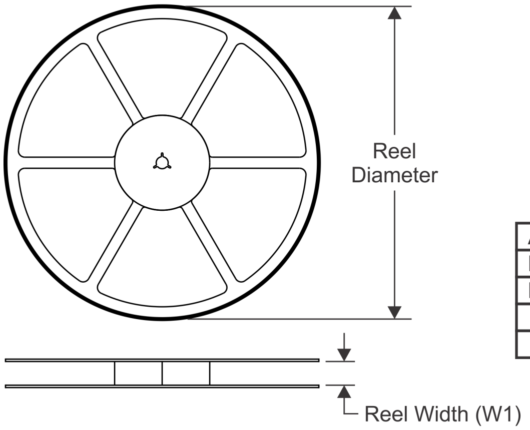
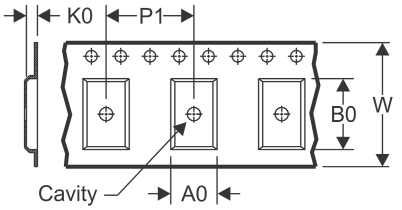
TAPE AND REEL INFORMATION

REEL DIMENSIONS

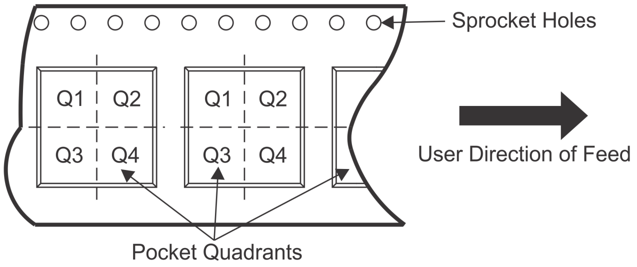


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

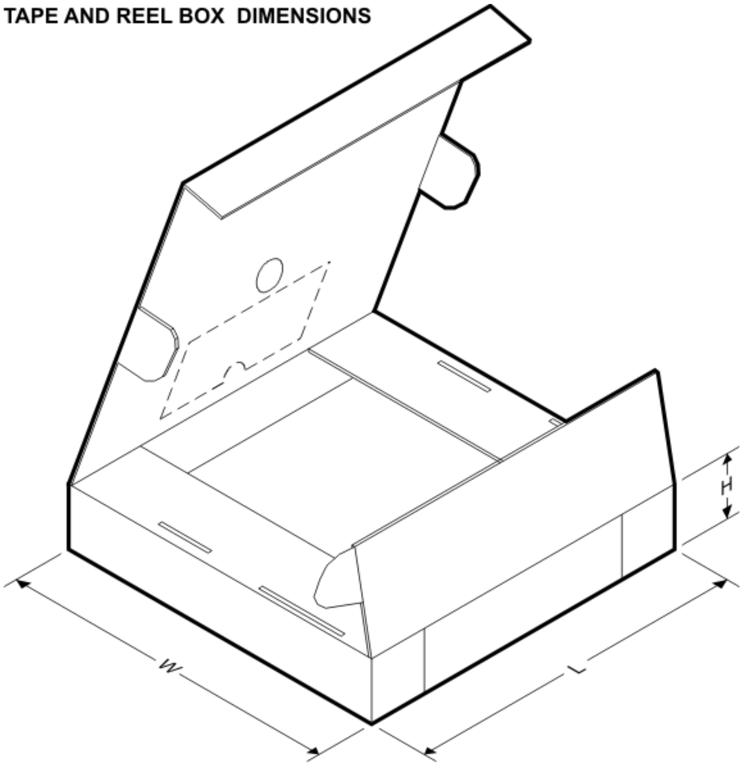
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP91200MTX/NOPB	TSSOP	PW	16	2500	330.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1

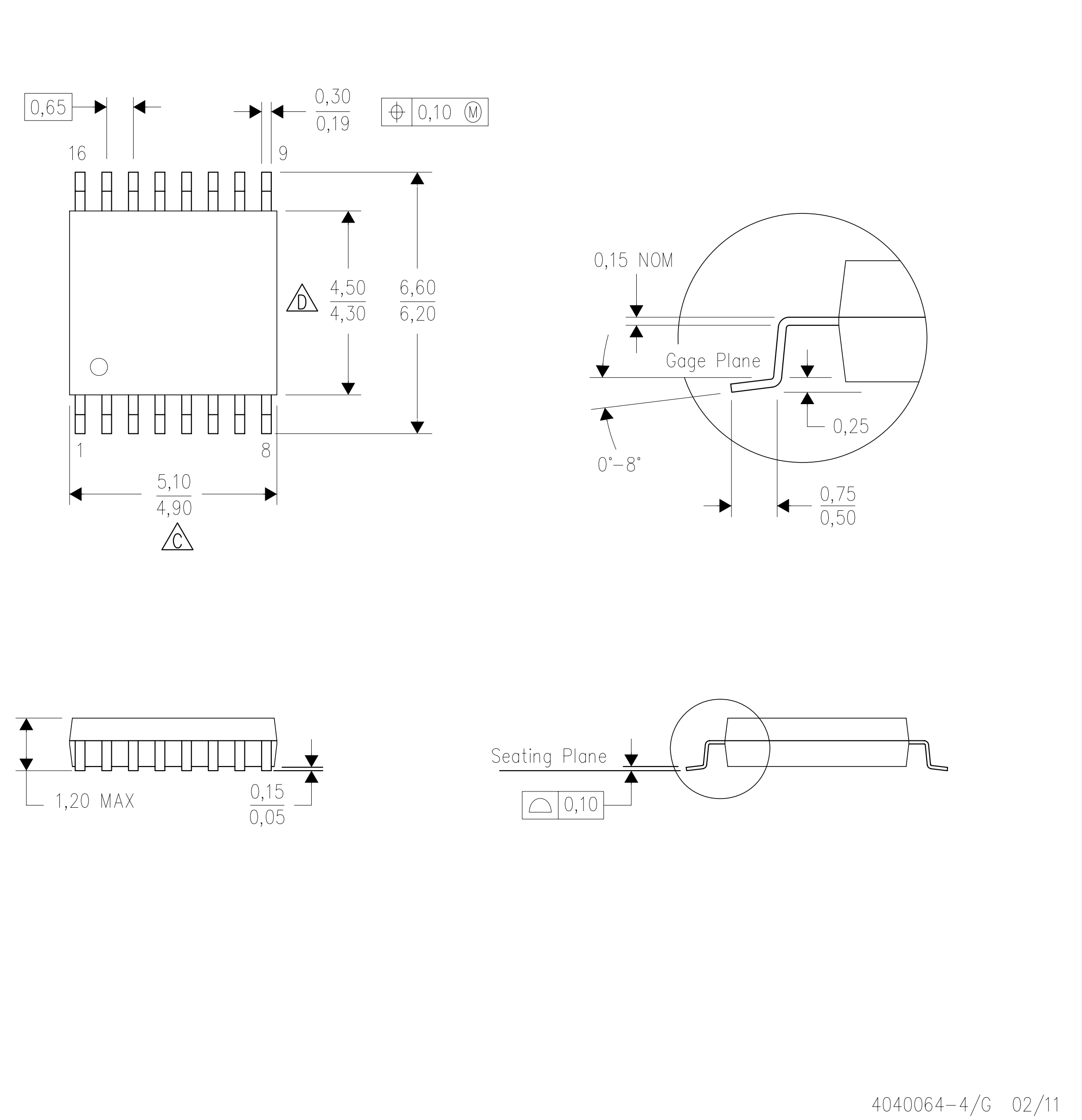
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP91200MTX/NOPB	TSSOP	PW	16	2500	367.0	367.0	35.0

PW (R-PDSO-G16)   PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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